HEATING ELEMENT FOR MICROFLUIDIC AND MICROMECHANICAL APPLICATIONS

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to microchip heaters for microfluidic and micromechanical applications, such as integrated chemical microreactors for decomposition and detection of bioorganic compounds such as DNA, ink-jet printer heaters for firing ink for printing purposes, optical switching based on vapor bubble formation to deflect a light beam, and optical switching based on liquid crystals.

Description of the Related Art

As is known, some fluids are processed at temperatures that should be regulated in an increasingly more accurate way, for example, when chemical or biochemical reactions are involved. In such situations, there is often also a need to use very small quantities of fluid, owing to the cost of the fluid, or to low availability.

This is the case, for example, of the DNA amplification process (PCR, i.e., Polymerase Chain Reaction process), wherein accurate temperature control in the various steps (repeated pre-determined thermal cycles are carried out), the need to avoid as far as possible thermal gradients where fluids react (to obtain here a uniform temperature), and also reduction of the used fluid (which is very costly), are of importance in obtaining good reaction efficiency, or even to make reaction successful. Microchip heaters are particularly suited for this application.

Other examples of fluid processing with the above-described characteristics are associated for example with implementation of chemical and/or pharmacological analyses, and biological examinations. Other situations that require a miniaturized heater that is one or more of more accurate, quicker reacting, more durable, longer-lived, more

controllable and less expensive to manufacture include ink-jet printers heaters and optical switching heaters to name a few.

At present, various techniques allow thermal control of chemical or biochemical reagents. In particular, from the end of the 1980s, miniaturized devices were developed, and thus had a reduced thermal mass, which could reduce the times necessary to complete the DNA amplification process. Recently, monolithic integrated devices of semiconductor material have been proposed, able to process small fluid quantities with a controlled reaction, and at a low cost (see, for example, U.S. Patent Applications 09/779,980, filed on February 8, 2001; 09/874,382 filed on June 4, 2001; and 09/965,128, filed September 26, 2001; all assigned to STMicroelectronics, S.r.l. and incorporated herein by reference).

These devices comprise a semiconductor material body accommodating buried channels that are connected, via an input trench and an output trench, to an input reservoir and an output reservoir, respectively, to which the fluid to be processed is supplied, and from which the fluid is collected at the end of the reaction. Above the buried channels, heating elements and thermal sensors are provided to control the thermal conditions of the reaction (which generally requires different temperature cycles, with accurate control of the latter), and, in the output reservoir, detection electrodes are provided for examining the reacted fluid. The heat is generated by supplying electric current to a metal heating element formed on a wafer comprising a semiconductor body with contact regions in electrical contact with the two opposite ends of the heating element and connected to a drive transistor, typically a MOSFET formed on the same wafer.

Current inkjet technology relies on placing a small amount of ink within an ink chamber, rapidly heating the ink and ejecting it to provide an ink drop at a selected location on an adjacent surface, such as a sheet of paper. Traditionally, ohmic resistors which heat up rapidly when current is passed therethrough have been used to provide the necessary temperature increase of the ink. See, for example, a detailed discussion of ink ejection in an article titled "Thermodynamics and Hydrodynamics of Thermal Ink Jets," by Allen et al., *Hewlett-Packard Journal*, May 1985, pp. 20-27, incorporated herein by reference.

Microchips are highly suited for miniaturized heater applications. Generally, present techniques for generating local heating in a microchip are based on ohmic resistors made of metal alloys, such as TaA1, HfB, ternary alloys, etc., or polycrystalline semiconductors. The heating resistor is driven by external circuitry or an integrated power MOSFET. In existing applications, such as thermal ink-jet printers, the heating resistor value is preferably higher than the MOSFET channel resistance (R_{ON} or R_{DS}) to minimize the parasitic effects and dissipate power in the heating resistor only. Normally, each power MOSFET occupies a large percentage of the chip area to minimize its R_{ON}.

One drawback with this arrangement is that the resistance of such ohmic resistors is fixed and cannot be modulated, thus limiting their flexibility. Other drawbacks are that ohmic resistors are subject to material degradation (such as oxidation, segregation, etc.), and electromigration, especially at high temperatures. These phenomena limit their lifetime and are a concern for the reliability of devices that incorporate them into their design.

Yet another drawback is power control. Ohmic resistors, which are either current or voltage driven, dissipate a power that is a quadratic function of the parameters. This results in poor control over their output, as small variations in current or voltage can cause significant fluctuations in power and temperature output.

The present invention provides a miniaturized heater that provides the desired characteristics for many microfluidic and micromechanical applications, while overcoming the drawbacks noted above, while providing other related advantages.

BRIEF SUMMARY OF THE INVENTION

The present invention resides in an integrated heater comprised of a semiconductor material, with at least one transistor formed in the semiconductor material and operable to generate heat, and an object to be heated positioned adjacent to the transistor to receive the heat generated by the transistor. In one embodiment disclosed, the object to be heated is a fluid chamber positioned adjacent to the semiconductor material.

The object to be heated may be, but is not limited to, a fluid chamber formed in the semiconductor material.

In some disclosed embodiments, the semiconductor material has a wall portion adjacent to the transistor to transmit heat generated by the transistor through the semiconductor wall portion. The heater further includes a body having wall portion positioned adjacent to and in sealing engagement with the semiconductor wall portion, such that the semiconductor wall portion and the body wall portion together define a fluid chamber as the object to be heated. The object to be heated may take forms other than a fluid chamber.

In some disclosed embodiments, the integrated heater further includes a thermally insulating barrier formed in the semiconductor material extending about the transistor to limit transmission in the semiconductor material of the heat generated by the transistor beyond the insulating barrier.

The heater may be manufactured with the semiconductor material extending laterally beyond the transistor to provide a lateral semiconductor portion, and the object to be heated may be positioned laterally adjacent to the transistor and adjacent to the lateral semiconductor portion to receive the heat generated by the transistor that is transmitted laterally to the lateral semiconductor portion. In at least one such embodiment, the heater has a dielectric layer extending over the semiconductor material with a window formed in a portion of the dielectric layer at a location adjacent to the lateral semiconductor portion, with the object to be heated positioned at the window to receive the heat generated by the transistor which passes through the window. The lateral semiconductor portion may have a wall portion to transmit heat to the object to be heated that is generated by the transistor and transmitted through the lateral semiconductor portion, and the heater may include a body with a wall portion positioned adjacent to and in sealing engagement with the lateral semiconductor wall portion, such that the lateral semiconductor wall portion and the body wall portion together define a fluid chamber as the object to be heated. In this embodiment, the thermally insulating barrier formed in the semiconductor material extends laterally outward of and about the transistor and the lateral semiconductor portion.

The integrated heater may be manufactured using a plurality of transistors formed in the semiconductor material and selectively operable to generate heat.

The integrated heater may be manufactured as a field effect transistor formed in a semiconductor substrate, with the transistor having a source region, a drain region and a channel region between the source and drain regions to conduct electric current, with the channel region having a resistance when conducting current to generate heat above a selected threshold. A dielectric layer is disposed on the channel region. A gate electrode is disposed on the dielectric layer to control the current conducted by the channel region. The object to be heated is positioned to receive the heat generated by the resistance of the channel region.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S)

In order to assist understanding of the present invention, preferred embodiments are now described, purely by way of non-limiting example, with reference to the attached drawings, wherein:

/ Figure 1 is a side elevational, cross-sectional schematic drawing of a MOSFET heater according to the invention;

/ Figure 2 is a side elevational, cross-sectional schematic drawing of a first alternative embodiment of the MOSFET heater of Figure 1 with a fluid chamber;

2 Figure 3 is a side elevational, cross-sectional schematic drawing of a second alternative embodiment of the MOSFET heater of Figure 1 with a fluid chamber formed fully in the semiconductor material;

3 Figure 4 is a side elevational, cross-sectional schematic drawing of a third alternative embodiment of the MOSFET heater of Figure 1 with a fluid chamber;

4 Figure 5 is a side elevational, cross-sectional schematic drawing of a fourth alternative embodiment of the MOSFET heater of Figure 1 with a fluid chamber and a thermally insulating trench extending about the MOSFET;

5 Figure 6 is a side elevational, cross-sectional schematic drawing of a fifth alternative embodiment of the MOSFET heater of Figure 1 with a fluid chamber using a

multiple source/drain MOSFET and a thermally insulating trench extending about the MOSFET;

6 Figure 7 is a side elevational, cross-sectional schematic drawing of a sixth alternative embodiment of the MOSFET heater of Figure 1 with a fluid chamber fed by a channel and a thermally insulating trench extending about the MOSFET;

7 Figure 8 is a side elevational, cross-sectional schematic drawing of a seventh alternative embodiment of the MOSFET heater of Figure 1 with a fluid chamber formed laterally offset from the MOSFET and on a front side of the MOSFET; and

8 Figure 9 is a side elevational, cross-sectional schematic drawing of an eighth alternative embodiment of the MOSFET heater of Figure 1 with a fluid chamber formed on a front side of the MOSFET immediately thereover and a thermally insulating trench extending about the MOSFET.

DETAILED DESCRIPTION OF THE INVENTION

As shown in the drawings for purposes of illustration, the present invention is embodied in an integrated heater, indicated generally by reference numeral 10, formed on a wafer 11. As shown in Figure 1, the wafer 11 has a substrate 12 of monocrystalline semiconductor material, for example silicon. The substrate 12 has been processed using well-known MOSFET manufacturing techniques to form a source region 14 and a drain region 16 of a MOSFET in the substrate toward an upper side or surface 18 thereof. A channel region 20 of the MOSFET is formed in the substrate 12 between the source and drain regions 14 and 16 to conduct electric current between the source and drain regions. The channel region 20 has a resistance R_{ON} or R_{DS}, indicated schematically by resistor symbol, to electric current so as to generate heat, indicated by arrows 22, when conducting electric current.

A dielectric layer 24, for example an oxide, is formed on the upper side of the substrate 12 and extends across the channel region 20. A gate electrode 26 of the MOSFET is formed on the dielectric layer 24 above the channel region 20 to control the current conducted by the channel region. The gate electrode can be composed of any

acceptable material, such as polysilicon, a polysilicon with a silicide layer thereon, or metal or any other conductive layer that is compatible with the process of the present invention. A metal silicide on top of a polysilicon is preferred in many instances because such a gate has a very low electrical resistivity with the advantage of a metal top layer for good thermal conductivity. The process technology and steps for forming such are well known. The MOSFET can be of any suitable type, such as LDMOS, VDMOS, etc.

A lower side or surface 28 of the substrate 12 has a portion thereof below the channel region 20 (at the back of the wafer 11) etched away or otherwise removed to reduce the thickness of the substrate in this area and to form a recess 29 in the substrate. The recess 29 defines at least in part forms a chamber 30 and serves as the object to be heated by the heat 22 generated by the channel region 20. The chamber 30 may be sized and shaped to receive a substance 32 to which the heat 22 transmitted into the chamber 30 is transferred. The chamber 30 is positioned close to the channel region 20 to receive the heat 22 generated by the channel resistance R_{DS} when the channel region is conducting electric current. The substrate 12 is removed when forming the chamber 30 so as to leave only a thin wall portion 34 thereof remaining below the channel region 20 in order to have the heat source (*i.e.*, the channel region) close to the substance 32 to be heated.

The lower side 28 of the substrate 12 has dielectric layer 36 formed thereon, such as by deposition or by being grown thereon. The dielectric layer 36 lines the portion of the lower side of the substrate that forms a part of the chamber 30. If the substance 32 to be received in the chamber 30 for heating is a fluid, the dielectric layer 36 may be selected as a material that provides protection to the substrate 12 against any harmful effects the fluid may have on the substrate if direct contact occurred. In the case of a fluid, the fluid in the chamber 30 can come into direct contact with the chamber walls and such is desirable to get the fluid close to the channel region 20 to have improved transfer of heat to the fluid. The heat 22 is transmitted through the dielectric layer 36 to the chamber 30 so the dielectric layer is selected with thermal properties sufficient to transfer the desired amount of heat. The heater 10 may be used to heat substances other than fluids, in which case the lower side 28 of the substrate 12 may be used as a heat transfer surface and shaped as appropriate

to contact the object to be heated, whether it be a flat object or a contoured object, with or without an intervening protective or other layer or other material.

As noted, the channel resistance R_{DS} (*i.e.,* source-to-drain resistance) of the channel region 20 generates the heat 22 and transfers that heat to the chamber 30 where the substance 32 is at least temporarily located so as to be heated. The channel region 20 generates the heat 22 when a sufficient voltage is applied to the gate electrode 26 to cause conduction in the channel region 20 between the source and drain regions 14 and 16, in a manner conventional with MOSFETs. The amount of heat 22 generated in a particular application can be controlled by the amount of voltage applied to the gate electrode 26 since the channel resistance R_{DS} in a MOSFET is a function of the gate voltage applied. A power MOSFET transistor can be used to achieve higher current conduction and an increased heating rating.

The channel resistance R_{DS} of the channel region 20 can be easily selected during fabrication of the MOSFET to produce a particular resistance value desired for a specific application, such as by varying the length and/or width of the channel region, the silicon doping used and/or the design layout so that the desired power is dissipated through the channel resistance R_{DS} when the MOSFET is on. It is noted that more normally doping of the channel region 20 is done in normal MOSFET production for the purpose of reducing the channel resistance, however, when the MOSFET is used as a heater, the doping is conducted to enhance/increase the resistance of the channel. A particular channel resistance R_{DS} is selected such that when the channel region 20 is conducting electric current, heat above a selected threshold is generated and transferred to the chamber 30 to heat the substance 32 in the chamber. The threshold is selected to supply the amount of heat desired to be transferred to the object to be heated or necessary to raise the temperature of the object to be heated or a substance to at least a desired temperature.

The MOSFET used in the heater 10 may be fabricated using conventional techniques to produce a channel resistance R_{DS} that may be from a few ohms to thousands of ohms, thus providing design flexibility. The operating temperature range of the channel resistance R_{DS} of the MOSFET can be between a few Celsius degrees and more than 1,000

Celsius degrees, thus providing sufficient heat for many microfluidic and micromechanical applications where local thermal gradients are required, such as to induce chemical reactions, or to produce mass and heat transportation such as to eject fluids or generate vapors. The substance 32 to which the heat 22 transmitted into the chamber 30 is transferred may be a fluid such as, but not limited to, ink, mixtures of organic materials, fluids for optical switching, and gases for environmental testing and medical applications, and the fluids mentioned in the Description of the Related Arts set forth herein, to name a few.

The heater 10 may be made easier and less expensively than known microchip heaters using ohmic resistors. Fewer mask processing steps are required and the expensive process control need to deposit and etch exotic resistor layers is eliminated. No expensive or exotic materials need be used. This results in simplified processing and less expense to fabricate the heater 10. Further, the cost is reduced since significant chip size reduction is achieved by the fact that the heater 10 does not require separate driving transistor and ohmic resistor assemblies be fabricated, both the driving transistor and the resistive element are combined together as the same element in the heater 10.

Increased reliability of performance for many applications will also be achieved using the heater 10. The resistors currently used for inkjet and optical switching applications have limited lifetime and fail for electromigration or physical damage (such as from cavitation) after a few billions of cycles. The lifetime of the channel region 20 of the heater 10 functioning to provide the channel resistance R_{DS} that produces the heat 22 should last for several years of operating conditions, which for inkjet printer applications is longer than the life of the printer. This is because the channel resistance R_{DS} is made from durable silicon crystal. This should allow the manufacture of inkjet printheads that are cheap and permanent, and do not need replacement during the normal lifetime of the inkjet printer.

The performance will also be increased for many applications when using the heater 10. This is in part due to the drastic reduction of parasitic resistance that is associated with the prior art microchip heaters using ohmic resistors. In the past when

using prior art microchip heaters using ohmic resistors, the channel resistance of the driving MOSFET was a main contributor to the parasitic resistance realized, in addition to the parasitic resistance of the metal traces that drive the transistor. With the heater 10, the "parasitic resistance" of the MOSFET becomes the heating element and parasitic effects are now primarily the low resistance metal traces that drive the MOSFET of the heater.

Another performance increase is achieved because the MOSFET transistor used in the heater 10 can be drawn as small as a few squared microns, thus allowing packing of a huge number of transistors on the same chip. For inkjet printers applications, this means that printheads can be manufactured which are capable of printing very high resolution pictures in one single pass.

Yet another performance increase results from the fact that a power MOSFET can be designed in such a way that at operational current/voltage, any fluctuation in these parameters has an insignificant impact on the dissipated power. Thus, the heater 10 is of particular interest for microreactor applications, such as chips for biological analysis, where lower temperatures and good temperature control are needed.

A first alternative embodiment of the heater 10 is shown in Figure 2. The heater 10 of Figure 2 has the same basic construction as the heater of Figure 1 except that the chamber 30 is in part formed by a body 38 that has a wall portion 40 that extends about the recess 29 in the substrate 12 on the back of the wafer 11. The wall portion 40 of the body 38 is positioned adjacent to and in sealing engagement with the substrate 12 at its lower side 28, with the dielectric layer 36 positioned therebetween. The wall portion 40 defines an open interior portion 42 that mates with the recess 29 to form the chamber 30, and defines an orifice 44 through which the substance 32 can pass, which in Figure 2 is shown as a fluid with a meniscus 46.

A second alternative embodiment of the heater 10 is shown in Figure 3. The heater 10 of Figure 3 has the same basic construction as the heater of Figures 1 and 2 except that the recess 29 formed in the substrate 12 on the back of the wafer 11 is shaped to form the entire chamber 30, including an orifice 48. If appropriate, the chamber 30 can be lined with a protective layer.

A third alternative embodiment of the heater 10 is shown in Figure 4. The heater 10 of Figure 4 has a different construction than the heaters of Figures 1-3 in that the MOSFET is made on a SOI (silicon on insulator) wafer 11' with the substrate 12 (such as silicon) having its lower side 28 engaging an oxide layer 50. The heat 22 generated by the channel region 20 is transmitted through the oxide layer 50 to the chamber 30 so the oxide layer 50 is selected with thermal properties sufficient to transfer the desired amount of heat to the chamber. The structure of Figure 4 can be obtained by using two separate wafers, one for the heating device and one for the chamber 30. The substrate for the chamber 30 can be any acceptable material for the chamber, including silicon, an organic polymer, sapphire, or any other suitable material. A layer 50 of an insulator is grown thereon that the back side of the wafer 12 is removed to a desired level and the wafer 11' is connected to the substrate 12. There are many acceptable techniques for doing this, one of which is described in pending application 854063.663, incorporated herein by reference.

In this third alternative embodiment, a body 52 made of silicon with a wall portion 54 defines the chamber 30 in conjunction with a lower side 56 of the oxide layer 50. The wall portion 54 of the body 52 is positioned adjacent to and in sealing engagement with the lower side 56 of the oxide layer 50. The wall portion 54 defines an orifice 58 through which the substance 32 can pass (not shown in Figure 4).

A fourth alternative embodiment of the heater 10 is shown in Figure 5. The heater 10 of Figure 5 has the same basic construction as the heater of Figure 4, using the SOI wafer 11' approach, except that a trench 60 is formed in the substrate 12 which is located laterally outward of and extends fully about the source and drain regions 14 and 16 and channel region 20. The trench 60 may be left empty or filled with an insulating material 62 such as silicon oxide. The trench 60 serves as a thermally insulating barrier to limit the lateral transfer of the heat 22 generated by the channel region 20 in the substrate 12, and as will be described below in greater detail, tends to contain the heat generated by the channel region and allow it to be better route the heat to the object to be heated. The trench 60 also serves to electrically isolate the MOSFET. The trench 60 projects fully between the dielectric layer 24 and the oxide layer 50.

A fifth alternative embodiment of the heater 10 is shown in Figure 6. The heater 10 of Figure 6 has the same basic SOI construction as the heater of Figure 5 except that it uses a multiple finger, power MOSFET with multiple source regions 14 electrically connected together, multiple drain regions 16 electrically connected together, and multiple gate electrodes 26 electrically connected together. There are, of course, multiple channel regions 20 between the adjacent source and drain regions. The trench 60 is located laterally outward of and extends fully about all of the source and drain regions 14 and 16 and channel regions 20 for the power MOSFET.

A sixth alternative embodiment of the heater 10 is shown in Figure 7. The heater 10 of Figure 7 has the same basic SOI construction as the heater of Figure 5 except that the substrate 12 and the body 52 extend laterally beyond the source and drain regions 14 and 16, the gate electrode 26 and the channel region 20, and a fluid channel 63 is provided in the body 52 which extends between a channel entrance aperture 63a and the chamber 30. A fluid flow, shown by arrow 65a, may enter the entrance aperture 63a and flow to the chamber 30 whereat the heat 22 generated by the channel region 20 is transferred to the fluid. The heated fluid can then exit the chamber 30 through the orifice 58, shown by arrow 65b. If the heater 10 is used as an inkjet printhead, the exiting heated fluid ink can be sprayed onto the paper or other material to be printed. The fluid channel 63 may also have an additional entrance aperture 63b in fluid communication with the channels of neighboring heaters, if desired.

A seventh alternative embodiment of the heater 10 is shown in Figure 8. The heater 10 of Figure 8 uses the same basic SOI construction; however, there is no chamber formed by the silicon body 52, which is a slab in this embodiment. Further, the chamber 30 is not located directly below the channel region 20 to receive the heat 22 generated thereby. Instead, the chamber 30 is located on the front of the wafer 11′ and is laterally offset from the MOSFET, as will be described below.

In particular, the substrate 12 has a lateral portion 64 that extends laterally beyond the source and drain regions 14 and 16, the gate electrode 26 and the channel region 20. The heat 22 generated by the channel region 20 is transmitted laterally to the lateral

substrate portion 64. In this seventh alternative embodiment, the oxide layer 50 is selected with thermal insulating properties and thickness to limit the amount of the heat 22 generated by the channel region 20 that is transferred through the oxide layer 50, *i.e.*, the oxide layer 50 serves as a thermal barrier. The insulating oxide layer 50, in conjunction with the trench 60, serve as thermally insulating barriers to limit the transmission of the heat 22 generated by the channel region 20 other than in the lateral direction to the lateral substrate portion 64, thus containing the heat generated by the channel region and allowing it to be better route the heat to the object to be heated.

In this seventh alternative embodiment of Figure 8, the dielectric layer 24 extends laterally over the lateral substrate portion 64, and an overlay dielectric layer 66 extends over the dielectric layer 50. The overlay dielectric layer 66 is selected with thermal insulating properties to limit the amount of the heat 22 generated by the channel region 20 that is transferred therethrough, and for passivation to protect the gate electrode 26 and the contacts 14a and 16a used for the source and drain regions 14 and 16. A window 68 is formed in the overlay dielectric layer 66 at a location laterally offset from the MOSFET and corresponding to the lateral substrate portion 64. A body 70 made of silicon with a wall portion 72 defines the chamber 30 with an inward opening 74 and an orifice 76 through which the substance 32 can pass, such as a fluid. The wall portion 72 of the body 70 is positioned adjacent to and in sealing engagement with the overlay dielectric layer 66, with the inward opening 74 of the chamber 30 in alignment with the window 68 so that the heat 22 generated by the channel region 20 which is transmitted laterally through the lateral substrate portion 64 will pass through the window and into the chamber.

An eighth alternative embodiment of the heater 10 is shown in Figure 9. The heater 10 of Figure 9 has the same basic construction as the heater of Figure 8 and has the chamber 30 is located on the front of the wafer 11′. However, instead of the substrate 12 and the body 52 extending laterally and providing a window in the overlay dielectric layer 66, in this eighth alternative embodiment the chamber 30 formed by the wall portion 72 of the body 70 has the inward opening 74 positioned immediately over the MOSFET. Further, the inward opening 74 has sufficiently large lateral sized to span the source and

drain regions 14 and 16, the gate electrode 26 and the channel region 20, and terminates above the trench 60 formed in the substrate 12 which is located laterally outward of and extends fully about the source and drain regions 14 and 16 and channel region 20. In such manner, the heat 22 generated by the channel region 20 is thermally blocked by the oxide layer 50 and the trench 60, and thus contained within the wall portion 34 of the substrate12 inward of the oxide layer 50 and the trench 60, and transmitted through the gate electrode 26 and the overlay dielectric layer 66 around the gate electrode. The heat 22 is then passed through the inward opening 74 and into the chamber 30. In this embodiment, the overlay dielectric layer 66 is selected with thermal properties which allow sufficient amount of the heat 22 generated by the channel region 20 to be transferred through the overlay dielectric layer as needed to supply the desired heat to the chamber 30 and to whatever substance may be therein.

To improve the efficiency of the heater 10, the gate electrode 26 used in this eighth alternative embodiment may be fabricated using a material that provides a desirable thermal conductivity for the application for which the heater is to be used. Also, the gate material may be selected to provide a long mechanical life. In an inkjet printhead, a material can be selected for the gate electrode 26 that can withstand the high pressures encountered with heated ink and the cavitation effect that is so damaging to prior art inkjet printhead component. The gate material can also be selected to avoid damage that might come from contact of the fluid with the gate electrode 26, should such occur. A metal, such as tantalum, tantalum alloy, aluminum and aluminum alloy are acceptable for the gate electrode 26. In this invention, it may be desirable to use a metal gate electrode and have the appropriate thickness gate dielectric, whether an oxide or nitride or sandwich thereof, to provide reliable, long-term operation for many applications.

The wafer 11 or 11′ on which the heater 10, or more likely many heaters of the design desired for the application, may also contain MOSFETs or other circuitry that serves to control the heater MOSFETs as well as perform other functions. By putting the heater MOSFETs and the other MOSFETs on the same wafer or chip that is produced therefrom, cost savings and size advantages can be achieved. In such an arrangement, the

heater MOSFETs and the other MOSFETs would be geometrically isolated from each other sufficiently that the channel regions of the two types of MOSFETs can be processed differently, with the channel region 20 of the heater MOSFETs being fabricated to enhance its channel resistance R_{DS} so as to produced the desired heat.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.